REMARKS/ARGUMENTS

1. Rejection of claims 1 and 9:

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuda et al. (US 2002/0015126). Reasons of rejection are cited in page 2-3 of above-mentioned Office Action.

Response:

Claims 1-9 are cancelled, and are no longer in need of consideration.

2. Rejection of claims 1-9:

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 2004/0095538). Reasons of rejection are cited in page 2-3 of above-mentioned Office Action.

Response:

Claims 1-9 are cancelled, and are no longer in need of consideration.

3. Rejection of claims 10-17:

Claims 10-17 are rejected under 35 U.S.C 103(a) as being unpatentable over Kida et al. (US 2004/0041976) in view of Tsuda et al (US 2002/0015126).

Response:

Applicants have amended claim 10 in this response. All amendments are based on original Fig.4 of the present application. Please refer to claim 10 and Fig.3-4. Fig.4 shows a plan view of a pixel region of an MVA LCD panel. An electrode patterned comprising a first electrode 82a and two second electrode 82b positioned in the pixel region. **The first electrode pattern 82a is parallel to the data line 88,** and the second electrode patterns 82b are perpendicular to the first electrode pattern 82a. The MVA LCD panel has **a plurality of**

slits 80 that are parallel to the first electrode pattern 82a. The protrusions 78 of the MVA LCD panel are parallel to the slit 80. Most importantly, **the protrusions in the pixel region are positioned above the first electrode 82a**.

In Kida's invention, Fig.5 shows *the protrusions 24 and the slit 16a are positioned in an arrow shape respectively and cross the capacity bus line 11b in an oblique angle*. Therefore, the protrusions 24 and the slits 16a are not parallel to the capacity bus line 11b, or the data bus line 13. In addition, as shown in Fig.6, *the protrusions 24 are disposed above the pixel electrodes 16*, not above the capacity bus line 11b.

In Tsuda's invention, Fig.1 shows that the capacitance bus line 8 are perpendicular to the auxiliary capacitance branch lines 9. *The protrusions 18 are arranged in an arrow shape and cross the capacitance bus line 8 and the auxiliary capacitance branch lines 9 in oblique angle.*

According to Kida's invention and Tsuda's invention, those skilled can construct an MVA LCD panel in which the protrusions cross the H-shaped electrode pattern **in oblique angle** and are positioned above the pixel electrode. However, the MVA LCD panel of the present invention has the first electrode pattern **parallel to** the data line, and further comprises the protrusions **parallel to** the first electrode pattern. In addition, the protrusions are positioned above the first electrode and are parallel to the slit. In comparison with the cited references, the light leakages close to the protrusions are covered by the electrode patterns positioned under the protrusions according to the instant application. Apparently, the structure of the MVA LCD panel of the present invention is different from prior references or combinations thereof. Therefore, those skilled in the art cannot simply combine the prior references to obtain the MVA LCD panel of the present invention.

In regard to claim 16, the electrode pattern of the MVA LCD panel can be used as a dummy circuit. Please refer to Fig.6-7 and corresponding [0028]. While the data line 88 is disconnected unexpectedly, the second electrode patterns 82 are cut apart. And two shorting points 94 are formed in the intersections of the data line 88 and the second electrode patterns 82 by laser irradiation, so that the data lines 88 and the second electrode patterns 82b are

electrically connected. And accordingly, **the voltage signal is delivered to each pixel via the first electrode pattern 82a and the second electrode pattern 82b. Therefore, the electrode pattern of the MVA LCD panel can be used as a dummy circuit of the data lines 88.** As for Tsuda's invention, the capacitance bus line 8 and the auxiliary capacitance branch lines 9 are positioned in the pixel. If a defect is occurred in the right-sided drain bus line 7, those skilled in the art may consider using the capacitance bus line 8 as substitute circuit. However, the signal from the right-sided drain bus line 7 will be delivered to the left-sided drain bus line 7. Therefore, *the capacitance bus line 8 and the auxiliary capacitance branch lines 9 cannot be used as the dummy circuit of the drain bus line 7.*

In regard to claim 17, the critical dimension of the protrusions is less than that of the electrode pattern. And consequently, **the light leakage close to the protrusion is effectively covered by the electrode patterns**. Compared to the present invention, *Kida and Tsuda never expect the occurrence of light leakage*. The solution of preventing light leakage cannot be taught or suggested by Kida and Tsuda.

Thus, claim 10 should be allowable over Kida and Tsuda. Claims 11-17 are dependent on claim 10 and should be allowable if claim 10 is found allowable. Reconsideration of claims 10-17 is respectively requested.

4. Introduction to new added claims 18-27:

Claims 18-27 are added according to Fig. 3-5 of the present invention.

Claim 18 describes the electrode pattern are arranged in I-shape that is illustrated in Fig. 4 and [0025] of the present invention. Claim 18 is dependent on claim 10, and consideration of claim 18 is requested.

Claims 19-27 describe that a MVA LCD panel based on Fig. 3 and 5, and are illustrated in [0021-0025]. Claim 19 describe an MVA LCD panel comprising a first substrate, a second substrate, a plurality of data lines, a plurality of electrode patterns, a dielectric layer, a liquid crystal layer, a common electrode layer, and a plurality of protrusions. The electrode patterns further comprise a first electrode pattern and two second electrode patterns perpendicular to

the first electrode. **The first electrode is perpendicular to the data line.** The protrusions are arranged parallel to and alternately with each slit. In addition, **the protrusions located in the pixel region are positioned above the first electrode pattern**, respectively. In the cited reference, the protrusions and the slit are positioned in an arrow shape respectively and cross the first electrode pattern in an oblique angle. Therefore, the protrusions and the slits are not parallel to the capacity bus line, or the data bus line 13. In addition, none of the cited reference mentions that the first electrode pattern are perpendicular to the data line and the protrusions are positioned above the first electrode pattern.

Claims 20-24 are dependent on claim 19, and are illustrated in [0021-0022] and [0024]. Claim 25 is dependent on claim 24, and is illustrated in [0028]. In the present invention, the electrode patterns can be served as dummy circuit to substitute the data line while the data line disconnected unexpectedly. Comparing the present invention, the electrode patterns in the cited reference cannot be used as redundant circuit to deliver the signal to the same pixel region. Claim 26 describes the critical dimension of the protrusions is less than that of the electrode pattern, and is illustrated in [0025]. Furthermore, the light leakage close to the protrusions can be covered by the electrode patterns, and the MVA LCD panel of the present invention does not require the black matrix being disposed above the protrusions. Claim 27 describes the electrode pattern is arranged in H-shape and is illustrated in Fig.5 and corresponding [0026]. Claims 20-27 are dependent on claim 19 and consideration of claims 20-27 is requested.

According to above reasons, claims 19-27 should be allowable. Acceptation and consideration of claims 19-27 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: September 08, 2006

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)